Tools to Debug “Dead” Boards

Hardware Prototype Bring-up

Ryan Jones
Senior Application Engineer
Corelis
Webinar Outline

- What is a Dead Board?
- Prototype Bring-up & Debug Cycle
- Existing Test Tools
- Corelis Structural & Emulation Test Tools
- Case Study – Complex TI Based Target
“Dead” generally refers to a board that does not respond, initialize or power-up to an expected state. Failure modes can typically be broken down into two categories: hardware and software.

**HARDWARE FAULTS**
- Power Related Fault
- Structural Fault
- Device Fault
- Timing Problem

**SOFTWARE FAULTS**
- Buggy Code
- Memory Initialization
- Stack Overflow
- Self Modifying Code
Prototype Bring-Up Cycle

- Visually check correct component installation
- Verify no shorts on power rails to ground
- Apply current-limited power to the board, ensure nothing gets hot, verify voltage levels
- Load basic boot code and functional code to verify CPU and peripheral operation

DEAD BOARD
Engineering Toolbox

- There are many tools that can assist in the debug process.
- Having the most efficient tool for the job saves engineering time.
- Knowing which tool to use at the right time is key.

Multi-Meter
Oscilloscope
Logic Analyzer
Bus Analyzer
Real-Time Trace
Debugger
In-Circuit Emulator
Corelis Toolbox

- Corelis directly replaces many traditional debug tools by providing automated test generation and low level diagnostic information saving valuable engineering time and effort.
- **Structural testing** identifies physical faults such as broken circuit traces, solder bridges and cold solder joints.
- **Emulation testing** verifies DSP operation and exercises peripheral interfaces at intended design speeds.
JTAG Architecture

Main Building Blocks of a JTAG Device

- JTAG Interface Pins
- Test Data Registers
- Instruction Register
- TAP Controller
JTAG Scan-Chain

Boundary-Scan Without Boundaries™
JTAG Test Vectors

- **Stimulus:**
  - 10001
  - 10010
  - 10100
  - 11000

- **Response:**
  - Short: HLLL L
  - Open: HH H H H

**Boundary-Scan Without Boundaries™**
JTAG Benefits

- JTAG provides the capability to test interconnects on a PC-board without physical test probes or test fixtures
- Does not require the board to be in a bootable state for fault diagnostics
- JTAG allows In-System Programming of devices such as Flash, CPLDs, FPGAs and Serial EEPROMs
JTAG Advantages

- Automatic test generation removes engineers from having to create elaborate test cases
- Fast test times
- Net/Pin level diagnostics
- JTAG helps identify board problems up front meaning general purpose tools like oscilloscopes and voltage meters are used less
- Test vectors can be reused in production
JTAG Emulation Test

JET uses a DSP’s JTAG debug port to perform:

- DSP initialization
- At-speed functional testing of DSP peripherals (memory, I/O)
- In-System-Programming (ISP) of flash devices
JET Benefits

- Does not require the board to be in a bootable state for fault diagnostics
- Embedded tests are downloaded and run from on-chip DSP memory at-speed
- Provides testability on all DSP addressable components by exercising their functionality
- In-system programming at theoretical speeds reduces time waiting for code to download
JET Advantages

- Automated test development for DSP initialization, memory and flash
- Device level diagnostics
- Customized diagnostic messages
- JET rigorously exercises all external memory locations before execution of any boot code
- Test vectors can be reused in production
# Combining JTAG & JET

<table>
<thead>
<tr>
<th>Feature</th>
<th>JTAG Test</th>
<th>Emulation Test</th>
<th>Combined Test</th>
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</thead>
<tbody>
<tr>
<td>Structural coverage</td>
<td>Very good</td>
<td>Good</td>
<td>Excellent</td>
</tr>
<tr>
<td>Functional coverage</td>
<td>Low</td>
<td>High</td>
<td>High</td>
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<tr>
<td>Programming (ISP) time</td>
<td>Average</td>
<td>Excellent</td>
<td>Excellent</td>
</tr>
<tr>
<td>Test time</td>
<td>Fast</td>
<td>Fast</td>
<td>Fast</td>
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<tr>
<td>Test points required</td>
<td>Very few</td>
<td>Very few</td>
<td>Very few</td>
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<tr>
<td>Test development</td>
<td>Automatic</td>
<td>Semi Auto</td>
<td>Auto/Semi</td>
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<tr>
<td>Diagnostics</td>
<td>Excellent</td>
<td>Average</td>
<td>Excellent</td>
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</tbody>
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JTAG & JET Fault Coverage

- JTAG Pin Connectivity; Noisy Signals
- Opens, Shorts & Stuck-At Conditions
- DSP Initialization
- Component Discovery and Identification
- Bad Memory Locations
- Flash Communication Problems
- Timing Problems
**Case Study — Complex TI Target**

- Board includes twenty-six TI DaVinci™ processors
- Board includes other JTAG and non-JTAG components
- JTAG components include a PowerPC CPU and two FPGAs
- Corelis JTAG tools are able to perform full interconnect and basic memory pin testing
- JET to the rescue...JET emulation testing identified crosstalk and signal integrity issues on SDRAM memories that JTAG scans did not detect
Benefits of Applying Boundary-Scan for Production Test

- No need for test fixtures.
- Integrates product development, production test, and device programming in one tool/system.
- Engineering test and programming data is reused in Production.
- Fast test procedure development.
- Preproduction testing can start the next day when prototype is released to production.
- Dramatically reduces inventory management – no pre-programmed parts eliminates device handling and ESD damage.
- Eliminates or reduces ICT usage time – programming and screening.